What is claimed is:

1. A semiconductor apparatus comprising:

a MIS transistor, wherein

a gate electrode of said MIS transistor is continuously formed to a position above a bypass film made of an insulation film through which a leak current is able to easily flow as compared with a gate insulation film of said MIS transistor under the same voltage level, said gate electrode being formed as well as on the gate insulation film of said MIS transistor.

2. A semiconductor apparatus according to claim 1, wherein said bypass film is made of the same material as that of said gate insulation film and the thickness of said bypass film is smaller than that of said gate insulation film.

3. A semiconductor apparatus according claim 1, wherein said bypass film is arranged in such a manner that a leak current in said film does not flow under a driving voltage or flows to an amount with which the operation of a circuit is not adversely affected.

4. A semiconductor apparatus according to claim 1, wherein an active region of said MIS transistor and a region of said bypass film are disposed independently.

5. A semiconductor apparatus according to claim 1, wherein a region of said bypass film is provided below a contact portion between said gate electrode of said MIS transistor and a metal wiring layer.

6. A semiconductor apparatus according to claim 1, wherein a region of said bypass film is provided adjacent to an active region of said MIS transistor.

7. A semiconductor apparatus according to claim 1, wherein a region of said bypass film is provided within a channel of said MIS transistor.

8. A semiconductor apparatus according to claim 1, wherein a region of said bypass film is formed to traverse a part of a channel of said transistor and a high-concentration region is formed in a channel below the region of said bypass film.

9. A method of manufacturing a semiconductor apparatus comprising the steps of:

forming a bypass film from an insulation film through which a leak current is able to easily flow as compared with a gate insulation film of a MIS transistor and forming a gate electrode which is continued to a position above said bypass film; and

performing a work process while performing

destaticization through said bypass film.

10. A method of manufacturing a semiconductor apparatus according to claim 9, further comprising the steps of:

selectively etching a gate insulation film of a region forming said bypass film to make the same thin after said gate insulation film of said MIS transistor has been formed; and

forming said gate electrode is formed to have a pattern continued from a region of said MIS transistor to a portion above said bypass film.

11. A method of manufacturing a semiconductor apparatus according to claim 9, further comprising the steps of:

forming a first gate insulation film of said MIS transistor, then selectively etching off said first gate insulation film of a region forming said bypass film and forming a second gate insulation film which will become said bypass film; and

then, forming said gate electrode to have a pattern continued from a region of said MIS transistor to a portion above said bypass film.

12. A solid state image device having a pixel composed of one MOS transistor, comprising:

a bypass film made of an insulation film through which a leak current is able to easily flow as compared with a gate insulation film, said bypass film being formed between a wiring

for connecting each gate electrode of a MOS transistor forming the pixel and a drain region.

13. A method of manufacturing a solid state image device comprising the steps of:

forming a bypass film through which a leak current is able to easily flow as compared with a gate insulation film, between a wiring for connecting each gate electrodes of a MOS transistor forming the pixel and a drain region, and

carrying out a work process is performed while performing destaticization through said bypass film.